#3

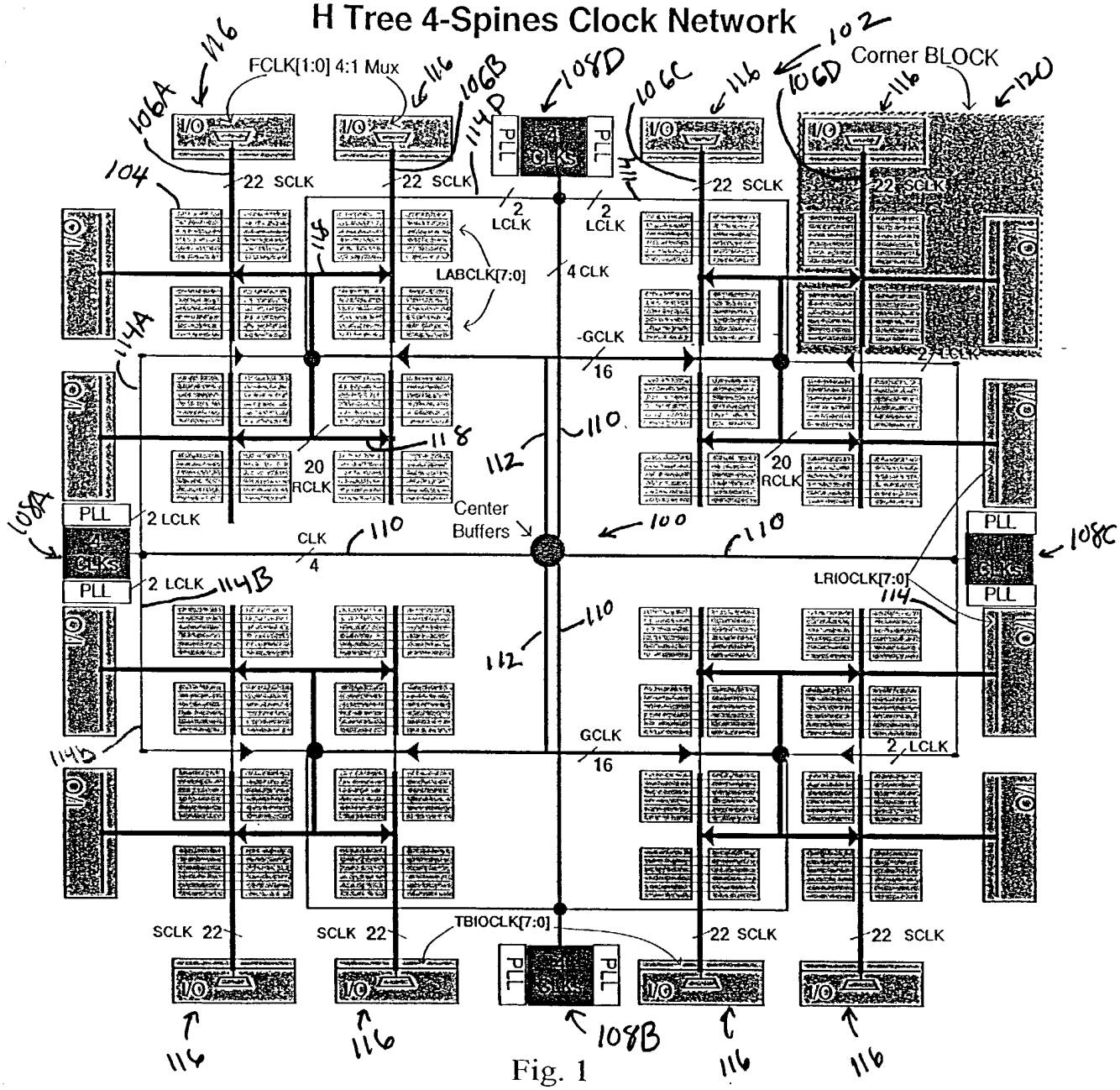
H Tree 4-Spines Clock Network
FCLK[1:0] 4:1 Mux
Corner BLOCK
22 SCLK
2 LCLK
LABCLK[7:0]
4 CLK
GCLK
16
20 RCLK
Center Buffers
CLK
4
PLL
4 CLKs
LRIOCLK[7:0]
TBIOCLK[7:0]
I/O
100
102
104
106A
106B
106C
106D
108A
108B
108C
108D
110
112
114A
114B
114C
114D
114P
116
118
120

Fig. 1

H Tree 2-Spines Clock Network

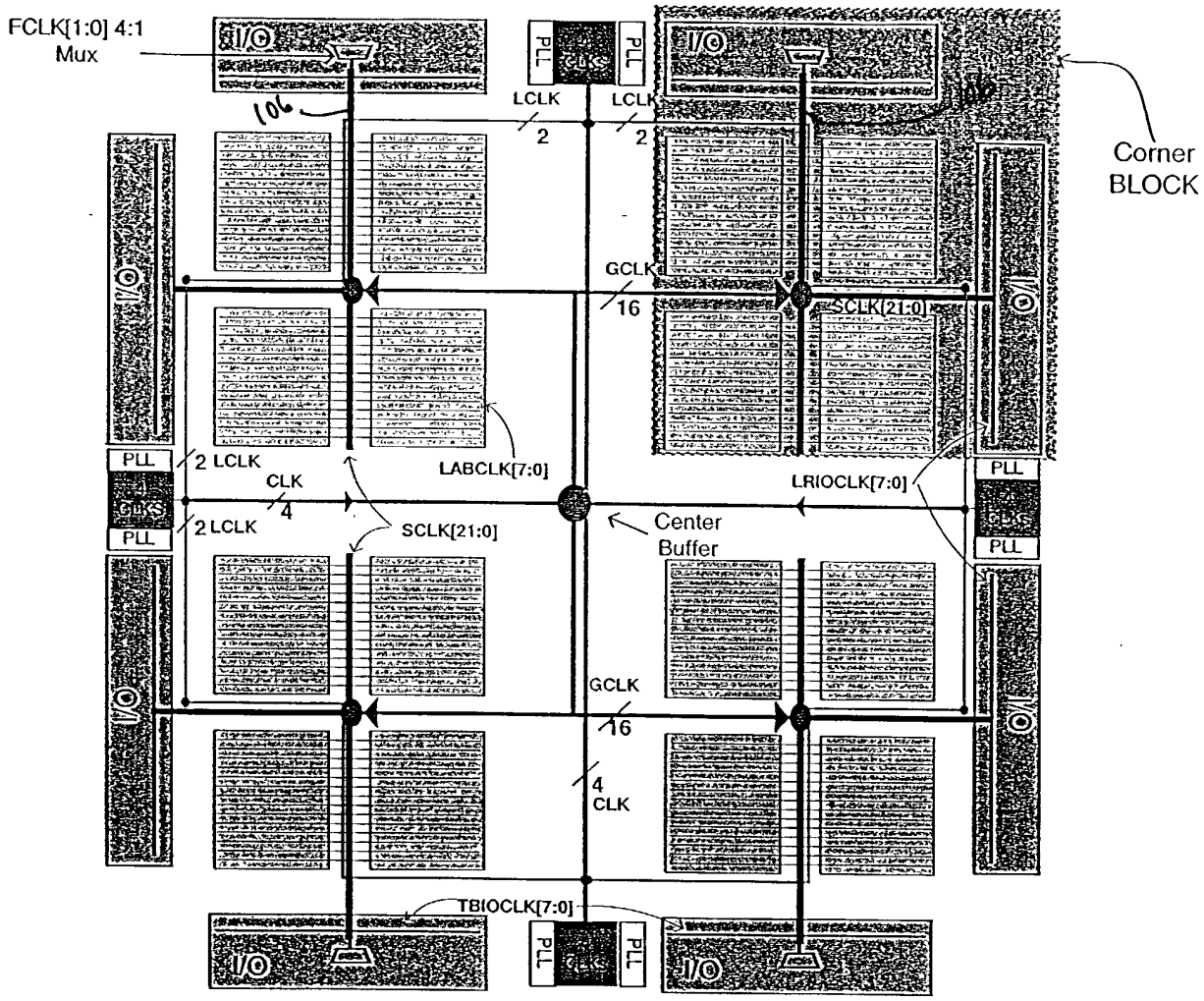

Fig. 2

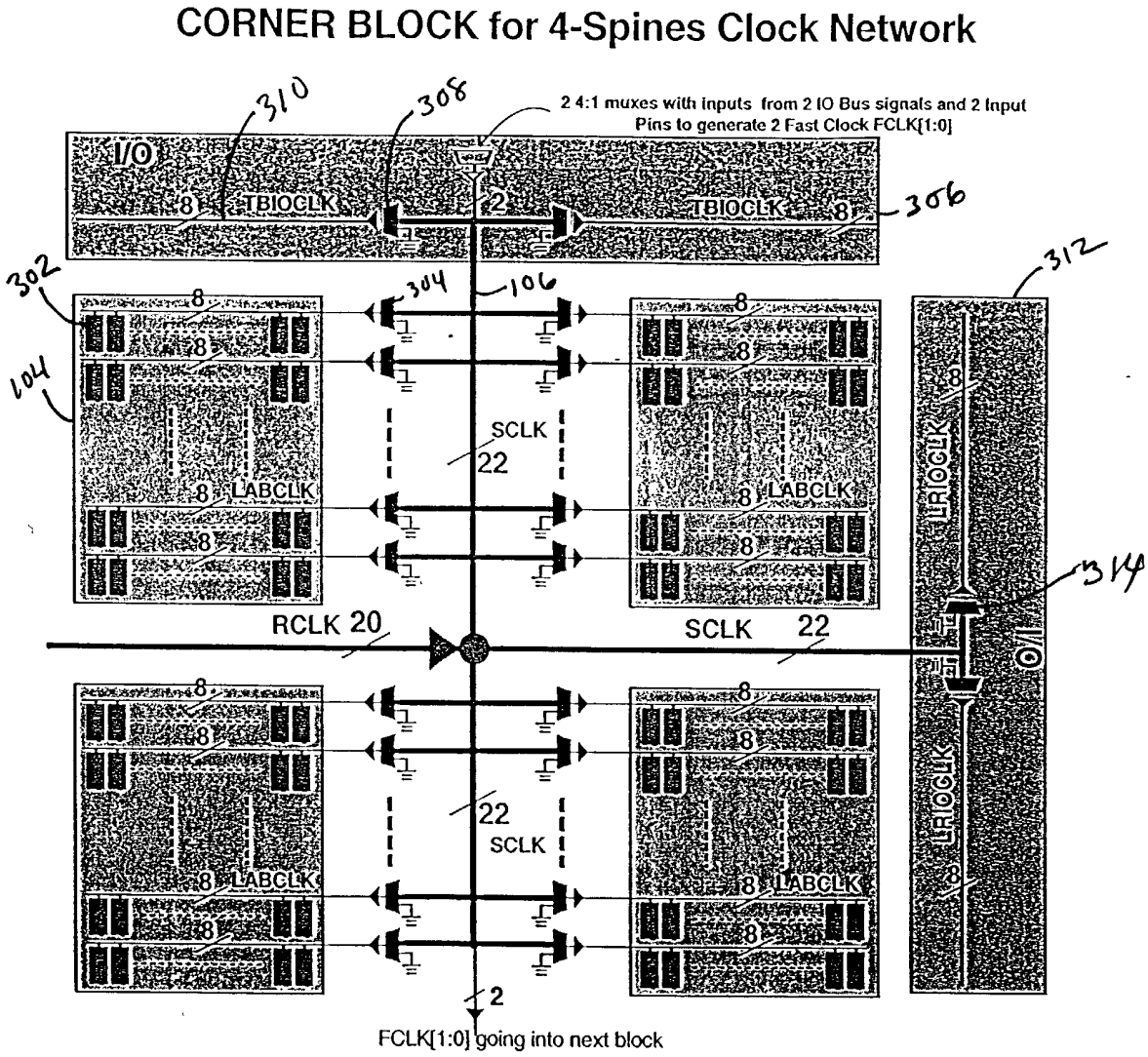

Fig. 3

CORNER BLOCK for 2-Spines Clock Network

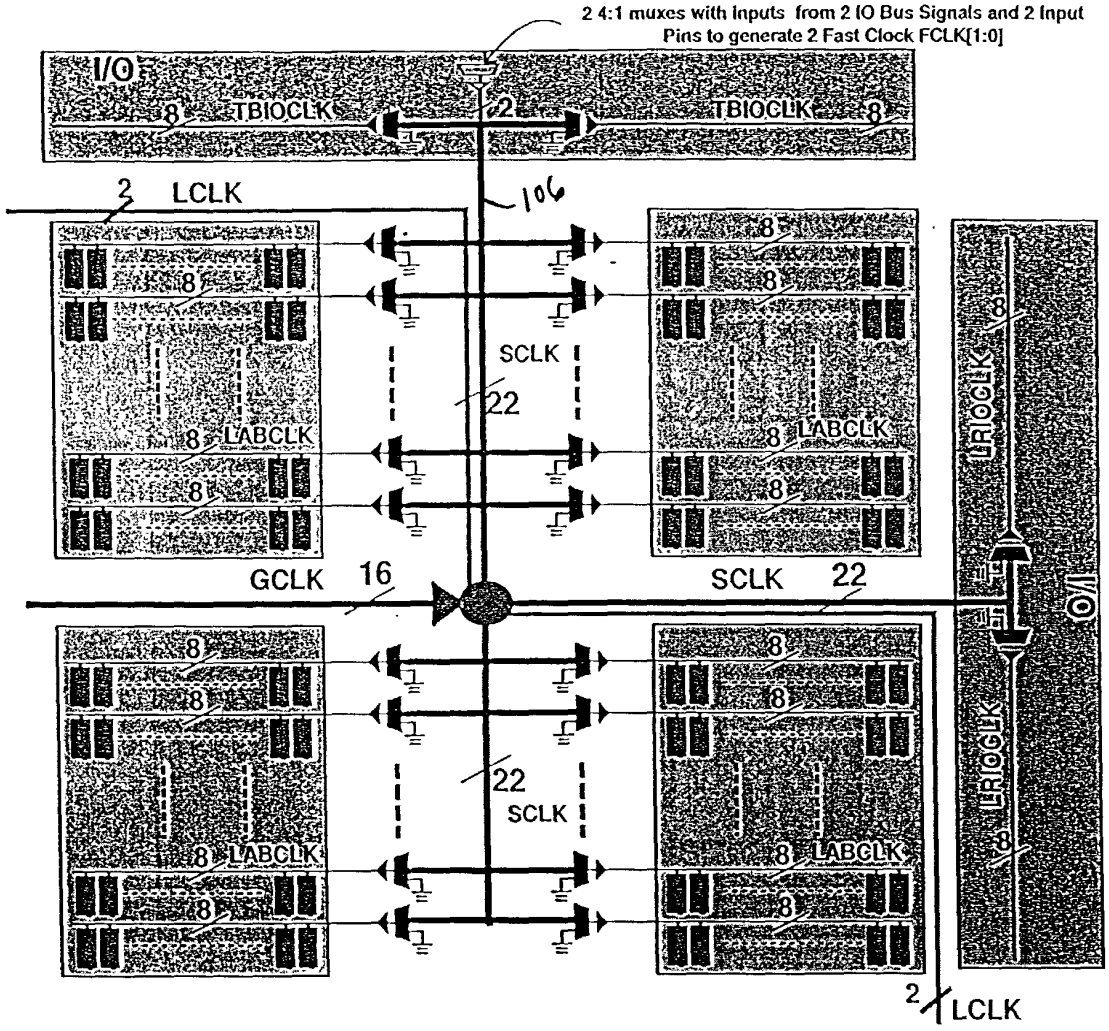

Fig. 4

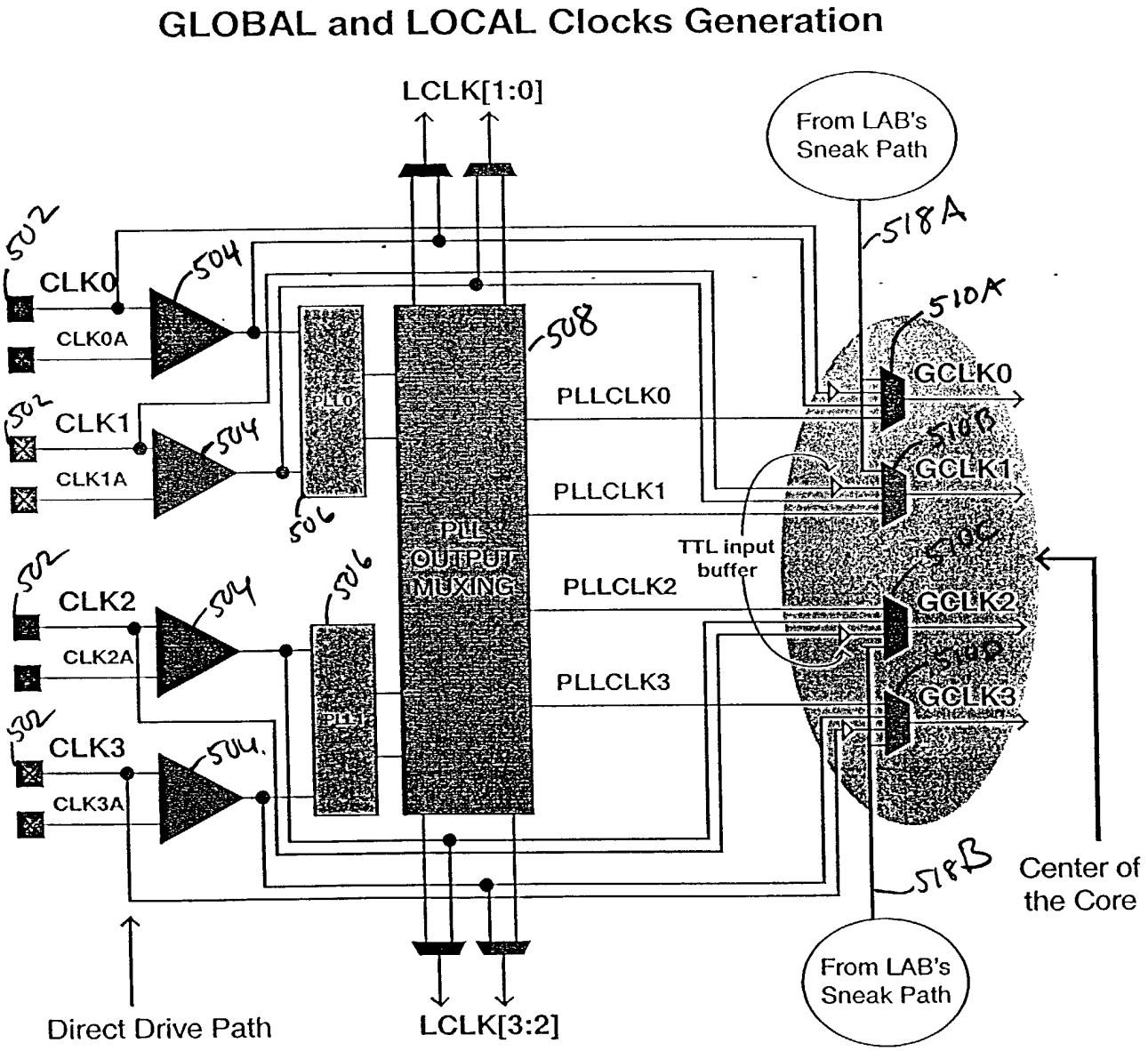
GLOBAL and LOCAL Clocks Generation
LCLK[1:0]
From LAB's Sneak Path
502
CLK0
CLK0A
504
CLK1
CLK1A
CLK2
CLK2A
CLK3
CLK3A
506
PLL0
PLL1
PLL OUTPUT MUXING
508
PLLCLK0
PLLCLK1
PLLCLK2
PLLCLK3
TTL input buffer
518A
510A
GCLK0
510B
GCLK1
510C
GCLK2
GCLK3
518B
Center of the Core
From LAB's Sneak Path
Direct Drive Path
LCLK[3:2]

Fig. 5

Generation of Global Clocks GCLK[15:0]

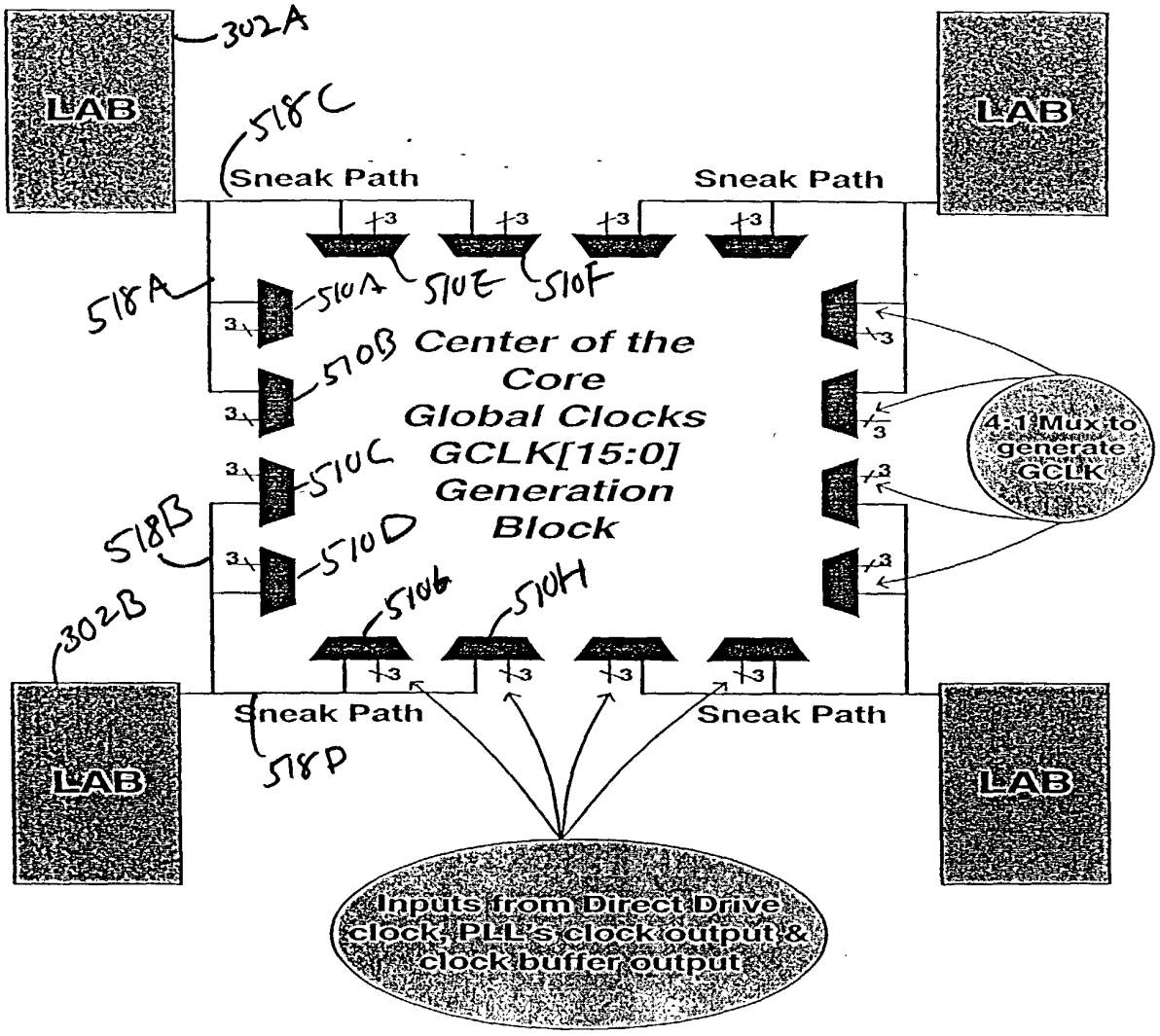

Fig. 6

Power Bus Segmentation for CLOCKs

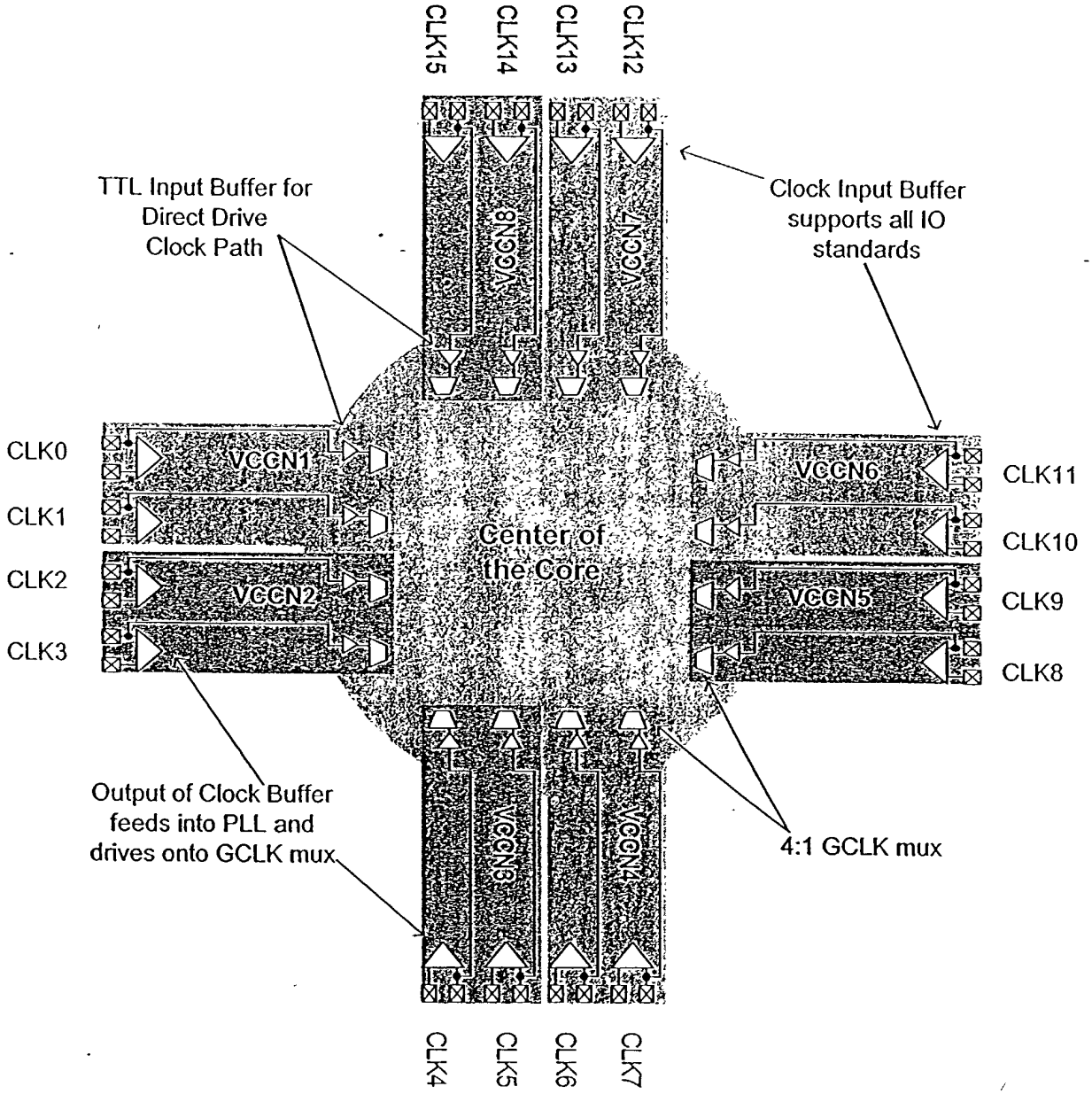

Fig. 7